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APPLICATION FOR LETTERS PATENT

FOR

LOW CAPACITANCE ESD-PROTECTION STRUCTURE UNDER A BOND PAD

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LOW CAPACITANCE ESD-PROTECTION STRUCTURE UNDER A BOND PAD

Field of the Invention

[0001] The present invention relates generally to semiconductor integrated circuits, and more particularly to protection of the semiconductor integrated circuits from electrostatic discharge (ESD).

Background of the Invention Technology

[0002] Modern electronic equipment uses digital semiconductor integrated circuits for operation thereof. The digital semiconductor integrated circuits receive inputs from various sources, *e.g.*, pushbuttons, sensors, *etc.*, and have outputs that control operation of the equipment based upon the various inputs thereto. The inputs and outputs of the semiconductor integrated circuits may be subject to undesirable high voltage electrostatic discharge (ESD) in addition to the desired input or output signal level. The ESD, characterized by fast transient high voltage discharges, may be from static electricity generated by a user of the equipment, equipment handling, power supply voltage transients and the like.

[0003] Semiconductor integrated circuits are becoming functionally more capable and are operating at faster speeds. The increased functional capability is the result of higher transistor count in each integrated circuit, thereby allowing the operation of more sophisticated software and/or firmware to produce the many features available in the equipment. The faster operating speeds further enhance the operation of the equipment. In order to keep integrated circuit die size within a reason cost, the electronic circuits therein must be more densely concentrated in as small an area as possible, thus the many transistors making up the electronic circuits within the integrated circuit must be made as small as possible. As these transistors

become smaller and smaller, the spacing of the parts of each transistor, *e.g.*, source, gate, drain, becomes smaller, as does the dielectric thickness of the insulation between these parts. The extremely thin dielectric is very susceptible to damage by excessive voltages present in an ESD event. Also, as operational speeds increase, the need for low capacitance structures becomes more important.

[0004] Various voltage protection circuits have been used to limit the peak voltage at an input and/or output of an integrated circuit. Attempts have been made to incorporate ESD protection within the integrated circuit, but are not very effective and/or require a significant amount of area within the integrated circuit die, and may add unacceptable additional capacitance to the circuit node being protected.

[0005] Therefore, what is needed is an ESD protection circuit integral within the integrated circuit die that is effective is protecting sensitive input and/or output circuits and has low capacitance.

SUMMARY OF THE INVENTION

[0006] The invention overcomes the above-identified problems as well as other shortcomings and deficiencies of existing technologies by providing an ESD-protection structure located substantially under an integrated circuit bond pad, having low capacitance and able to absorb high current ESD events. An ESD-protection structure is located substantially under an integrated circuit bond pad in which is formed a low capacitance structure by inserting a forward diode between the bond pad and the ESD clamp circuit. Placing the ESD-protection structure under the bond pad eliminates parasitic substrate capacitance and a parasitic PNP transistor is formed from the inserted forward biased diode.

[0007] The invention comprises a semiconductor structure of adjacent alternating P+ and N+ diffusions located substantially under the bond pad to be ESD protected. The P+ diffusions may be shaped in squares, rectangles, stripes and the like (other shapes and are also contemplated herein), and may be connected to the bond pad with conductive vias through an insulating layer located between the bond pad and the P+ and N+ diffusions. The N+ diffusions are arranged adjacent to and surround the P+ diffusions. The N+ diffusions are insulated from the bond pad by the insulating layer. An N- well is located in a P- well of the integrated circuit and substantially under the N+ and P+ diffusions. The N+ diffusion partially overlaps the edge of the N- well into the P- well. An outer portion of the N+ diffusion, the portion overlapping the N- well, is within the P- well.

[0008] Another N+ diffusion encircles the N+ diffusion surrounding the P+ diffusions. The another N+ diffusion is in the P- well and a field oxide is located between the N+ diffusion and the another N+ diffusion. A field transistor (NPN) is thereby formed with the N+ diffusion being the transistor collector, the P- well being the transistor base and the another N+ diffusion being the emitter. The another N+ diffusion (emitter) may be connected to ground by a conductive connection, *e.g.*, metal or low resistance semiconductor material. The P- well may be a P- substrate of an integrated circuit, or the P- well may be a P- well in an N- substrate of an integrated circuit.

[0009] Capacitance of the above described ESD-protection structure is minimal because the only capacitance seen by the bond pad is the P+ diffusions to N- well and the N+ and P+ diffusions/N+ diode junction capacitance. The bond pad metal to the P- well capacitance is substantially reduced by the ESD-protection structure being mostly under the bond pad.

[0010] The invention ESD-protection structure clamps a voltage transient through the NPN field transistor in combination with the parasitic PNP transistor. The NPN and PNP transistors work together to increase the ESD-protection response through the multiplication of the gains of both transistors. The bond pad voltage to ground increases until the N+ diffusion to P- well diode breaks down (conducts). The bond pad voltage will therefore be a diode drop above this breakdown voltage. Then the NPN field transistor snaps back. The ESD-protection clamping operation is further enhanced by the vertical PNP parasitic structure formed from the P+ diffusions, the N- well and the P- well. As the transient current flows through the NPN field transistor, a portion of the current flows directly to the P- well due to the presence of the aforementioned vertical PNP parasitic structure.

[0011] A technical advantage of the invention is very little additional capacitance to the bond pad. Yet another technical advantage is high current clamping of ESD transients. Another technical advantage is enhanced ESD clamping by the vertical PNP parasitic structure. Another technical advantage is reduce size for an ESD structure. Yet another technical advantage is isolating the bond pad from the substrate capacitance.

[0012] Features and advantages of the invention will be apparent from the following description of the embodiments, given for the purpose of disclosure and taken in conjunction with the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

[0013] A more complete understanding of the present disclosure and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawing, wherein:

[0014] Figure 1a illustrates a schematic diagram of a sectional elevational view of an ESD-protection structure, according to an exemplary embodiment of the invention;

[0015] Figure 1b illustrates a schematic diagram of a plan view of the ESD-protection structure shown in Figure 1a;

[0016] Figure 1c illustrates a schematic diagram of a plan view of another ESD-protection structure; and

[0017] Figure 2 illustrates a schematic circuit diagram of the ESD-protection structure of Figure 1.

[0018] While the present invention is susceptible to various modifications and alternative forms, specific exemplary embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0019] Referring now to the drawings, the details of exemplary embodiments of the present invention are schematically illustrated. Like elements in the drawing will be represented by like numbers, and similar elements will be represented by like numbers with a different lower case letter suffix. P- refers to lighter doped p-silicon, P+ refers to heavier doped p-silicon, N- refers to lighter doped n-silicon, and N+ refers to heavier doped n-silicon, wherein p-silicon has a plurality of positive immobile silicon ions, and n-silicon has a plurality of negative immobile silicon ions.

[0020] Referring to Figure 1, depicted is a schematic diagram of an ESD-protection structure, according to an exemplary embodiment of the invention. Figure 1a illustrates a sectional elevational view, Figure 1b illustrates a plan view of the ESD-protection structure and Figure 1c illustrates a plan view of another ESD-protection structure. A semiconductor integrated circuit comprises many transistors, inputs and output. The ESD-protection structure shown in Figure 1 may be advantageously used for both inputs and outputs of the integrated circuit to protect the delicate transistors connected thereto.

[0021] The ESD-protection structure of Figure 1, generally represented by the numeral 100, is located substantially under an integrated circuit bond pad 114. The ESD-protection structure 100 comprises alternating P+ diffusions 126 and N+ diffusions 128, located substantially under the integrated circuit bond pad 114. The P+ diffusions 126, may be arranged in stripes (see Figure 1b) or in alternating squares (see Figure 1c), and are connected to the bond pad 114 with conductive vias 116 through an insulating layer 124 located between the bond pad 114 and the P+ diffusions 126 and the N+ diffusions 128. The N+ diffusions 128 are

adjacent to and surround the P+ diffusions 126. Other shapes for the P+ diffusions 126 may be used and are contemplated herein. An N+ diffusion 128a surrounds the N+ diffusions 128 and P+ diffusions 126, and ties together the N+ diffusions 128 so as to form a continuous N+ diffusion 128 completely around each of the P+ diffusions 126. The N+ diffusions 128 may be formed as one N+ diffusion 128 during fabrication of the integrated circuit. The N+ diffusions 128 are insulated from the bond pad metal by the insulating layer 124. The P+ diffusions 126 are connected to the bond pad 114 by conductive vias 116. An N- well 130 is located substantially under the N+ diffusions 128 and the P+ diffusions 126. The surrounding N+ diffusion 128a partially overlaps the edge of the N- well 130 below. The integrated circuit substrate 132 comprises P- semiconductor material that behaves as a P- well. The ESD structure of the invention may also be formed within a P- well located in an N- substrate of an integrated circuit. An outer portion of the N+ diffusion 128a, the portion overlapping the N- well 130, is within the P- well 132. Another N+ diffusion 128b encircles the N+ diffusion 128a that ties together the N+ diffusions 128. The another N+ diffusion 128b is in the P- well 132 and a field oxide 122 may be located between the N+ diffusion 128a and the another N+ diffusion 128b. In addition, the N+ diffusions 128 may be connected together by conductive vias connected together by conductive paths (not shown).

[0022] An NPN field transistor 104 is formed with the N+ diffusion 128a being the transistor collector, the P- well 132 being the transistor base and the another N+ diffusion 128b being the transistor emitter. The another N+ diffusion 128b (emitter) may be connected to ground by a conductive connection, *e.g.*, metal or low resistance semiconductor material (*e.g.*, vias 118 and conductors 120, one or more of each). A PNP transistor 102 is formed with the

P+ diffusions 126 being the transistor emitter, the N- well 130 being the transistor base and the P- well 132 being the transistor collector. A diode 108 is formed between the N- well 130 and the P- well 132. Generally, the P- well 132 is coupled to ground (and/or a negative rail of a power source) and functions like a resistance to ground, generally represented by resistor 110.

[0023] Capacitance of the above described ESD-protection structure 100 is minimal because the only capacitance seen by the bond pad 114 is the P+ diffusions 126 to N- well 130 which forms a diode junction capacitance. The bond pad 114 to the P- well 132 capacitance is substantially reduced because the ESD-protection structure 100 being mostly under the bond pad 114.

[0024] Referring to Figure 2, depicted is a schematic circuit diagram of the ESD-protection structure of Figure 1. The invention ESD-protection structure 100 clamps a voltage transient on the bond pad 114 substantially the same as would be typical of a NPN field transistor or other semiconductor structures. The bond pad voltage to ground increases until the N+ diffusion to P- well diode 108 breaks down (conducts). The bond pad voltage will therefore be a diode drop above this breakdown voltage. Then the NPN field transistor 104 snaps back. The ESD clamping operation is enhanced by the vertical PNP parasitic structure (transistor 102) formed from the P+ diffusions, the N- well and the P- well. As the transient current flows through the NPN field transistor 104, a portion of the current flows directly to the P- well due to the presence of the aforementioned vertical PNP parasitic structure (transistor 102).

[0025] The invention, therefore, is well adapted to carry out the objects and attain the ends and advantages mentioned, as well as others inherent therein. While the invention has been depicted, described, and is defined by reference to exemplary embodiments of the invention,

such a reference does not imply a limitation on the invention, and no such limitation is to be inferred. The invention is capable of considerable modification, alternation, and equivalents in form and function, as will occur to those ordinarily skilled in the pertinent arts and having the benefit of this disclosure. The depicted and described embodiments of the invention are exemplary only, and are not exhaustive of the scope of the invention. Consequently, the invention is intended to be limited only by the spirit and scope of the appended claims, giving full cognizance to equivalents in all respects.